Session (4) Advanced EDA using AI/ML at Synopsys

Time	23 January, 2023 (Tuesday)
Location	Room 110/111
Chair	Kyumyung Choi (Seoul National University)

1. AI-Driven Solution for DFT Optimization

Speaker: Soochang Park (EDA Group, Synopsys, Korea)

Abstract:

In the industry of semiconductor design, configuring optimal specifications for a design is becoming challenge due to numerous inter-dependent design parameters. Specifically, in design for testability (DFT), it is more demanding to predict the quality of test pattern in advance since it is generated through automatic test pattern generation (ATPG) step after DFT IP is implemented. Thus, such flow innately requires long iteration run-time and computing resources for designers. In frond-end of design implementation step, ways to improve ATPG quality of results (QoR) can be adjusting DFT specifications and applying automatic test-point insertion (TPI). However, DFT specifications should be considered within design limitations and hierarchical design guidelines, and TPI solutions might increase area overhead. To find the recipe of DFT for optimal ATPG results while considering the design circumstances, the ML applied solution of Synopsys is suggested as a promising solution to automates the process and eventually to replaces human resources. In conducted experiments, integrating two different steps from DFT insertion to ATPG is enabled, so that the ML solution can automate the flow and learn the relation of DFT recipe and ATPG QoR. The experimental results not only show outstanding results in terms of ATPG QoR, but also successfully show that the constraints of synthesis can be reflected in accordance with the user's intention.

2. Optimization of PDN and DTCO using Synopsys Machine Learning Framework

Speaker: Kyoung-In Cho (EDA Group, Synopsys, Korea)

Abstract:

In the realm of sub-nanometer technology nodes, the semiconductor industry faces the challenge of fulfilling increasingly complex application demands while adhering to stringent power, performance, and area (PPA) requirements. A major hurdle is the mismatch between metal pitch and cell height reduction, leading to heightened routing congestion and hindering effective chip size reduction. Although adding more metal

layers can mitigate this issue, it substantially raises production costs and expands the design space, especially when considering IR-drop during physical implementations. Design-Technology Co-Optimization (DTCO) emerges as a vital strategy to bypass physical scaling limits and enhance transistor density, performance, and power efficiency. However, it significantly broadens the design scope in physical implementations, as chip designers must integrate technology-related variables with existing design parameters in the early technology stage. To address these challenges, we advocate for the integration of Machine Learning (ML) to identify and optimize technical parameters. ML demonstrates exceptional potential in fine-tuning complex parameters. Specifically, Synopsys DSO.ai (Design Space Optimization AI), a pioneer in applying ML within the Electronic Design Automation (EDA) sector, shows promising results. Our experiments using Synopsys DSO.ai successfully identify an optimal metal pitch that minimizes IR-drop impact and efficiently determine suitable parameters for DTCO.